7/9/03

REMARKS

The claims are claims 1 to 12.

The application has been further amended to update the status of the co-pending patent application cited at page 1. Additional minor errors on page 19 have been corrected.

Claims 1 and 4 have been amended to further distinguish over the reference Bhattacharya. New claim 5 recites the preferred coding of the first and second logic states as disclosed in the application at page 18, lines 24 to 25. New claims 6 to 12 are apparatus claims to the apparatus illustrated in Figure 8 and disclosed in the application at page 18, line 31 to page 20, line 2.

Claims 1 to 4 were rejected under 35 U.S.C. 102(e) as anticipated by Bhattacharya, U.S. Patent No. 6,378,090. The Applicant respectfully submits that while it is possible that the hardware disclosed in Bhattacharya may be employed to practice the method of this invention, Bhattacharya fails to anticipate the method claimed in claims 1 to 4.

Claim 1 recites subject matter not anticipated by Bhattacharya. Claims 1 recites "supplying to the test data input port for communication to the boundary-scan architecture a serial signal having a number of bits greater in number than a number of bits of the serial connection of the plurality of registers, each bit of said serial signal having a first logic state." Claim 1 further recites "following supply of said serial signal, supplying to the test data input port for communication to the boundary-scan architecture a single start bit having a second logic state opposite to said first logic state followed by a predetermined number of data bits." Thus claim 1 requires the serial signal having plural bits in the first logic state and the single start bit of the second and opposite logic state to be transmitted on the

serial connection via the test data input port. The FINAL REJECTION cites Figure 13, column 11, lines 31 et seq and column 13, lines 30 et seq as allegedly anticipating this subject matter. Bhattacharya states at column 3, lines 58 to 61:

> "FIG. 2 illustrates a-state diagram of test access port controller 121 as specified in the JTAG standard. All the signals illustrated are input at the test mode select pin 133 which are read at edges of the test clock."

By analogy all the signals illustrated in the similar Figures 12 and 13 are also the test mode select TMS signal. As clearly set forth in Bhattacharya at column 3, lines 40 to 57, the signal test data input TDI on pin 137 is the serial data signal and the signal test mode select TMS on pin 133 is a mode signal. Bhattacharya teaches that Figure 13 illustrates the condition of the test mode select TMS signal. Figures 1, 11, 15 and 17 of Bhattacharya clearly illustrated the test mode select TMS signal on pin 133 coupled to only respective tap controllers 121, 921, 1221 and 1421 and not to the serial connection of plural data registers claimed. Accordingly, any teaching in the cited portion of Bhattacharya corresponds to a different input than that claimed. Accordingly, claim 1 is allowable over Bhattacharya.

The FINAL REJECTION states at page 3, lines 13 to 15 regarding the Applicant's previous response concerning "supplying to the test data input port for communication to the boundary-scan architecture a serial signal having a first logic state for a number of cycles greater in number that a number of bits of the serial connection of the plurality of registers" that:

> "Although the claimed signal or data supplied to the port is not the same as the data in the Bhattacharya patent, the type of signal supplied is not claimed. Also, with an input port or pin, any type of data or signals can be put on the input to the circuit."

The Applicant respectfully disputes this statement. Claim 1 recites the nature of the data "having a first logic state" and its duration "for a number of bits greater in number that a number of bits of the serial connection of the plurality of registers." The Applicant respectfully submits that this language clearly recites the "type of signal supplied" in this method claim. Further, claim 1 is a method claim and thus can be distinguished over the art based upon the "type of data or signals...put on the input to the circuit." Accordingly, claim 1 is allowable over Bhattacharya.

The FINAL REJECTION states at page 3, lines 18 to 20 regarding the Applicant's previous response concerning "supplying to the test data input port for communication to the boundary-scan architecture a start bit having a second logic state opposite to said first logic state" that:

> "in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., opposite start bit on the serial connection) are not recited in the rejected claim(s)."

The Applicant respectfully disputes this statement. Claim 1 recites "supplying to the test data input port for communication to the boundary-scan architecture a single start bit having a second logic state opposite to said first logic state." This language clearly sets forth the opposite start bit upon which the Applicant's argument depends. Thus claim 1 is allowable over Bhattacharya.

Claim 4 recites subject matter not anticipated by Bhattacharya. Claim 4 recites "supplying a serial signal having said first logic state to following registers in the serial connection of the plurality of registers for a predetermined number of bits and supplying to following registers in the serial

connection of the plurality of registers a single start bit having a second logic state opposite to said first logic state followed by said predetermined number of data bits." Claim 4 requires that the serial signal of the first logic state, the start bit of the second opposite state and the predetermined number of data bits be supplied to "the following registers in the serial connection of the plurality of registers." The FINAL REJECTION cites a portion of Bhattacharya teaching a serial connection of plural registers. This portion of Bhattacharya fails to teach the three different signals on the serial connection recited in claim 4. Particularly, the Applicant respectfully submits that Bhattacharya fails to disclose an opposite start bit on the serial connection. Accordingly, claim 4 is allowable over Bhattacharya.

The FINAL REJECTION states at page 3, line 17 to page 4, line 2 regarding the Applicant's previous response concerning "three different signals on the serial connection" that:

> "(5) see column 3, lines 18 et Seq. for serial connection and in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., opposite start bit on the serial connection) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)."

The Applicant respectfully submits that claim 4 does explicitly recite the three different signals. Claim 4 recites: 1) at lines 5 to 8 "supplying a serial signal having said first logic state to following registers in the serial connection of the plurality of registers for a predetermined number of bits"; at lines 8 to 10 "supplying to following registers in the serial connection of the plurality of registers a single start bit having a second logic state opposite to said first logic state"; and at lines 10 and 11

"said predetermined number of data bits." The Applicant respectfully submits that claim 4 thus recites the three signals of the argument that are not anticipated by Bhattacharya. Accordingly, claim 4 is allowable over Bhattacharya.

New claim 5 recites subject matter not made obvious by Bhattacharya. New claim 5 recites the first logic state is 1 and the second logic state is 0. Bhattacharya does not make this subject matter obvious.

New claims 6 to 12 are apparatus claims. The Applicant respectfully submits that Bhattacharya fails to make obvious: the start bit detector recites in claim 6; the selection of first and second logic states recited in claim 7; the bypass path recited in claim 8; or the alternative data output register and the start bit generator recited in claim 12. Accordingly, claims 6 to 12 are allowable.

The Applicant respectfully requests entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicant respectfully submits that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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